WHAT IS CLAIMED IS:

1. A display provided with a shift register circuit including a first circuit part comprising:

a first transistor of first conductivity type connected to a first potential side and turned on in response to a clock signal;

a second transistor of first conductivity type connected to a second potential side;

a third transistor of first conductivity type connected between a gate of said first transistor and said second potential; and

a high resistance connected between the gate of said first transistor and a clock signal line supplying said clock signal.

2. The display according to claim 1, wherein

said high resistance has a resistance value set such that the moment said first transistor of a predetermined stage of shift register circuit is switched from off state to on state may not overlap with the moment said first transistor of the shift register circuit two stages prior to the predetermined stage is switched from on state to off state.

3. The display according to claim 2, wherein

said high resistance has a value set such that said first

transistor of the predetermined stage of shift register circuit is turned on, after said first transistor of the shift register circuit two stages prior to the predetermined stage was turned off.

4. The display according to claim 3, wherein a signal corresponding to said first potential is output from said first circuit part through said first transistor, and

an output signal of said first circuit part of the predetermined stage of shift register circuit is switched from said second potential to said first potential, after an output signal of said first circuit part of the shift register circuit two stages prior to the predetermined stage was switched from said first potential to said second potential.

5. The display according to claim 1, wherein

said first circuit part further comprises a diode-connected fourth transistor connected between the gate of said first transistor and said clock signal line and having an on-resistance lower than that of said third transistor.

6. The display according to claim 5, wherein

said fourth transistor is a p-type field effect transistor.

7. The display according to claim 5, wherein

said fourth transistor has two gate electrodes electrically connected to each other.

8. The display according to claim 1, wherein

said first circuit part further comprises a fourth transistor connected between the gate of said first transistor and said clock signal line and turned on in response to a signal by which a period of on state which does not overlap with a period of on state of said third transistor is provided.

9. The display according to claim 8, wherein said fourth transistor is a p-type field effect transistor.

10. The display according to claim 8, further comprising a diode-connected fifth transistor connected between said fourth transistor and said clock signal line.

11. The display according to claim 10, wherein said fifth transistor is a p-type field effect transistor.

12. The display according to claim 1, wherein

a capacitor is connected between the gate and the source of said first transistor.

13. The display according to claim 1, wherein

said third transistor has a function of turning said first transistor off when said second transistor is in on state.

14. The display according to claim 1, wherein

at least said first transistor, said second transistor and said third transistor are p-type field effect transistors.

15. The display according to claim 1, wherein

at least said third transistor has two gate electrodes electrically connected to each other.

16. The display according to claim 1, wherein

said first circuit part is arranged on an output side of said shift register circuit, and

a second circuit part comprising said first transistor, said second transistor and said third transistor but not comprising said high resistance is arranged on an input side of said shift register circuit.

17. The display according to claim 1, wherein

said shift register circuit comprises a shift register circuit for driving a drain line to which a picture signal is supplied.

18. The display according to claim 17, wherein

said drain line driven by said shift register circuit has a function of supplying said picture signal to a display pixel comprising a liquid crystal.

19. The display according to claim 17, wherein

said drain line driven by said shift register circuit has a function of supplying said picture signal to display pixel comprising an organic EL element.